ABSTRACT

A technique is described for performing critical parameter analysis (CPA) of a semiconductor device (DUT) by combining the capabilities of conventional automated test equipment (ATE) with a focused optical beam scanning device such as a laser scanning microscope (LSM). The DUT is provided with a fixture such that it can be simultaneously scanned by the LSM or a similar device and exercised by the ATE. The ATE is used to determine pass/fail boundaries of operation of the DUT. Repeatable pass/fail limits (for timing, levels, etc.) are determined utilizing standard test patterns and methodologies. The ATE vector pattern(s) can then be programmed to "loop" the test under a known passing or failing state. When light energy from the LSM scanning beam sufficiently disturbs the DUT to produce a transition (i.e., to push the device outside of its critical parameter limits), this transition is indicated on the displayed image of the DUT , indicating to the user which elements of the DUT were implicated in the transition.